## ABSTRACT

Heightening of breakdown voltage of a trench gate type power MISFET is actualized without increasing the number of manufacturing steps. In the manufacturing method of the semiconductor device according to the present invention, p<sup>-</sup> type semiconductor region and p<sup>-</sup> type field limiting rings are formed in a gate line area simultaneously in one impurity ion implantation step so as to bring them into contact with a groove having a gate extraction electrode formed therein. Upon formation, supposing that the width of the gate extraction electrode disposed outside the groove is CHSP, and the resistivity of the n<sup>-</sup> type single crystal silicon layer 1B is  $\rho$  ( $\Omega$ ·cm), the CHSP is set to satisfy the following equation: CHSP  $\leq$  3.80 + 0.148 $\rho$ .